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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,505	04/24/2001	Brian W. Curran	POU920000107US1	5674

7590 10/29/2004

Lynn L. Augspurger
IBM Corporation
2455 South Road, P386
Poughkeepsie, NY 12601

EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,505	CURRAN ET AL.	
	Examiner	Art Unit	
	Magid Y Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is with reference to Application No. 09/841,505, filed 24 April 2001. Claims 1 – 9 are pending in this application.

Specification

2. The abstract of the disclosure is objected to because the Abstract should always end with a period (“.”). Correction is required. See MPEP § 608.01(b).

Claim Objections

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). Claim 5 is missing.

Misnumbered claims 6, 7, 8 and 9 have been renumbered 5, 6, 7 and 8

4. Claims 1 – 8 are objected to because of the following informalities:

- Claim 1, lines 4, 6, 8, 9 and13 delete "," and insert --;--.
- Claim 1, line 13, delete "(f)" and claim 1, line 17, delete "(h)".
- Claim 1, line 14, delete "(g)" and insert --(f)--.
- Claims 2 and 3, line 1, insert --, -- before "wherein".
- Claims 4, 5, 6, 7 and 8, line 1 insert --, -- before "whereby".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,724,250 to Kerzman et al. (hereinafter, "Kerzman"), in view of "Performance Analysis of Tapered Gate in PD/SOI CMOS Technology" to Hwang, et al (hereinafter, "Hwang"), published in Proceedings of Technical Papers, 2001 International Symposium on VLSI Technology, Systems and Applications, 18 – 20 April 2001, pp. 287 – 290.

7. Referring to claim 1, Kerzman teaches a logic synthesis method (Fig. 8, block 558) for reducing the delay of a timing critical path in a circuit (Fig. 8, blocks 578, 582 and 586) comprising the steps of: (a) selecting a gate in the timing critical path (col. 5, lines 7 – 40); (b) replacing gate with functionally equivalent gate (col. 5, lines 22 – 32); and (c) iteratively performing timing analysis of circuit to determine if replacing the gate will improve timing (Fig. 6, blocks 410, 414 and 426; see also Figs. 7 and 8). Kerzman cites all the claimed elements except for (d) the selection of a gate that is not an inverter in the critical timing path; and (e) the use of a "tapered" gate when a selection is made to replace a gate in a critical path. However, Hwang cites the performance analysis of tapered gates in the design and synthesis of state-of-the-art CMOS microprocessors. Hwang shows in his publication that tapered stacked gate designs (i.e., gates that have several stacked NMOS devices in series, and therefore not an inverter) can be faster than conventional CMOS designs. See pages 287 and 289; Tables 1 and 3. As stated by Hwang (page 287 – Introduction) stack ordering exploits the well-known fact that the switching of the top transistor is significantly faster than the switching of the bottom transistor in stacked configuration by placing the critical path signal on the top of the stack, representing the fourth dimension, and thus the delay/performance of the paths through the top transistor in stack configuration can be further improved by introducing these tapered gates. Thus, Hwang provides the motivation for combining these two disclosures. It would therefore be obvious to a person of

ordinary skill in the art at the time the invention was made to combine the teachings of Kezman and Hwang to obtain the same claimed inventions.

8. As per claims 2 and 3, see Kerzman, Fig. 9, blocks 704, 774; col. 24, lines 33 – 47, and Hwang – Tables 1 and 3, which respectively show the conventional (non-tapered gates with stacked devices of the same width), and the tapered gates (i.e., gates characterized by a stack of devices of different widths. Furthermore, as cited, the cell library consists of gates such as NAND, NOR, etc as claimed herein.

9. Referring to claim 4, see Hwang – Tables 1 and 3, which compare the delay through tapered and non-tapered gates, as claimed.

10. As per claim 5, see Hwang – Fig. 1; Tables 1 and 3, which show a plurality of tapered gates functionally equivalent to non-tapered gates, as claimed.

11. Referring to claim 6, see (5) – 98) above, as well as Kerzman – Figs. 6, 8 and 9, which show how gates in a critical timing path (such as tapered gates available for use) can be swapped for comparison with a timing analysis of the circuit as claimed.

12. As for claim 7, see claim 4 as well as Kerzman - Fig. 8, which disclose the elements of comparing delays through paths that contain tapered and non-tapered gates.

13. As per claim 8, see (5) - (10) above, as well as Kerzman – Figs. 3, 6 and 7, which disclose the logic synthesis method whereby the gate, which yields the shortest delay, is retained for the circuit, as claimed.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,397,169 to Shenoy et al. cites a process for synthesis and rough placement of an IC design, whereby a synthesis tool is used to generate a netlist according to HDSL user constraints and technology data.

U.S. Patent No. 4,827,428 to Dunlop et al. teaches a method and system for improving the design of an IC by iteratively analyzing the circuit and improving it with each iteration until a pre-selected constraint is met.

Pub. No. US 2001/0049814 to Matsumato et al. discloses an automatic logic design supporting method and apparatus capable of laying out a circuit of logic

synthesis result as to be able to satisfy delay constraints without changing the logic structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
06 October 2004

A. M. Thompson
Primary Examiner
Technology Center 2800